**Abstract**

A two-chip/single-die switch architecture and a method for accessing a DDR SDRAM memory store in a switching environment are presented. The two-chip/single-die architecture includes an internal memory storage block on the single-die, an external memory storage interface to a Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM), an external memory manager, and a packet data transfer engine effecting packet data transfers between an internal memory store and the external DDR SDRAM memory. The packet data transfer engine operates as an adaptation layer addressing issues related to employing appropriate: addressing schemes, granule sizes, memory transfer burst sizes, access timing, etc. The packet data transfer engine includes a minimal number of dual mode operational blocks such as: a queue manager, and adaptation receive and transmit blocks. The method relates to a packet data transfer discipline addressing random memory access latencies incurred in employing DDR SDRAM, using predictive bank switching to hide random access latencies, packet length dependent variable memory write burst lengths to minimize bank switching, and performing memory read and write operations during corresponding read and write windows. Advantages are derived from the a space-efficient two-chip/single-die switching node architecture implemented with a reduced amount of dual mode logic, and also from DDR SDRAM bandwidth utilization efficiencies.